Remarks:

In the Office Action mailed on March 26, 2010, the Examiner rejected Claims 1, 5-7, 10, 12-17, and 19 - 32. Claims 1, 12, 13, 14, 16, 17, 20 – 26, 29, and 30 are amended herein.

Claims 1 - 3, 5-7, 10, 12-17, 19-32 are pending in the application. Claims 2 and 3 have been withdrawn.

The Specification

In preparing arguments with respect to the art rejections made in the Office Action, Applicants discovered that a series of translation errors had occurred in translating the French priority application (PCT/FR99/02428). In particular, the words "sealed" and "sealing layer" are used in several places in the specification. These derive from the French word "sceller." While the English verb "to seal" is one translation of "sceller," in the context of the present invention a better translation would be "to bond" and variations thereof. Dr. Jerome Denis, a French speaker with relevant technical expertise as well as excellent English language skills, files herewith a declaration in which he declares that "to bond" and derived words there from is the preferred translation. Applicants have amended the specification accordingly. As "to bond" and words derived there from are the preferred translation of the original text, these amendments do not constitute addition of new matter.

Applicants further amend the specification to clarify that the various silicon layers presented therein are *monocrystaline* silicon layers. That a *monocrystaline* layer is intended may be inferred from several items in the specification as filed:

- With respect to the silicon substrate layer 12 it is stated "[t]his layer 12 has an active face 13 in which the circuits are integrated and a face opposite from said active face 13, i.e., the rear face 6" (Page 6, Lines 5 – 6). As integrated circuits that are created on silicon substrate layers are always

created on *monocrystaline* silicon, it may be inferred that the substrate 12 is *monocrystaline* silicon.

- With respect to the additional layer 14, it is stated that "the dopants 17 can be incorporated in the crystal lattice while *the* silicon crystal is being grown" (Page 8, Lines 7 – 9) thus implying one crystal, i.e., *monocrystaline* silicon.
- Further, with respect to the additional layer 14, it is stated that the additional layer is about 150μm (Page 6, Lines20 – 21) which is commonly the thickness of a wafer of *monocrystaline* silicon.
- On Page 7, Lines 8 – 14 contains a discussion of "*an* intrinisic silicon crystal" thereby implying a *monocrystaline* silicon.

From the foregoing it may be inferred with respect to both the substrate layer 12 and the additional layer 14 that these layers are *monocrystaline* silicon layers. Accordingly, the introduction of "monocrystaline" as a modifier to silicon in the specification does not constitue addition of new matter.

35 USC 103

Claims 1, 5-7, 20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (US 4,970,565, hereinafter Wu). Claims 6, 21 – 23, and 26 - 28 stand rejected under 35 USC 103(a) as being unpatentable over Wu, in view of Kuehnle (US 5,534,056, hereinafter Kuehnle). Claims 10, 12 – 13, 24 and 29 stand rejected 35 USC 103(a) as being unpatentable over Wu, in view of Kobachi, et al., (US 5,811,797, hereinafter Kobachi). Claims 14 – 17, 19 and 30 - 32 stand rejected 35 USC 103(a) as being unpatentable over Wu, in view of Ishikawa (US 5,394,014, hereinafter Ishikawa). Applicants traverse the rejections.

Claim 1

Claim 1 as amended recites:

"A chip for a chip-containing portable article comprising: a monocrystaline silicon substrate layer having an active face with circuits integrated therein defining a central processor unit and memories; and an additional layer of monocrystaline silicon that: is bonded to the active face of the monocrystaline silicon substrate layer by a bonding layer; covers at least part of said active face; and comprises physical means for providing physical protection against the action of electromagnetic radiation in the infrared range at a wavelength longer than 1 μm."

With respect to the additional layer of silicon the Examiner cites Wu's radiation shield or cover 18; of which Wu states "[alternatively, silicon substrate material polysilicon which has been p-typed doped, such as with boron, may be used." Applicants have amended Claim 1 to recite that the additional layer is a monocrystaline silicon layer. Monocrystaline silicon and polysilicon are very different materials. Polysilicon, or more correctly, polycrystalline silicon is a material consisting of small silicon crystals. "In single crystal silicon, also called monocrystal, the crystal lattice of the entire sample is continuous and unbroken with no grain boundaries. Large single crystals are exceedingly rare in nature and can also be difficult to produce in the laboratory." Polycrystaline silicon, en.wikipedia.org/wiki/Polycrystalline_silicon, Accessed and Printed on September 28, 2010 (attached hereto as Exhibit A). *Id.* Polycrystaline silicon, in contrast, is composed of a number of smaller crystals or crystallites. Polycrystaline silicon is a material consisting of multiple small silicon crystals. "Polycrystalline cells can be recognized by a visible grain, a "metal flake effect"."

Thus, Wu's disclosure of a polysilicon alternative for the shield or cover 18 is not equivalent to Applicant's monocrystaline silicon element.

Furthermore, Applicants claim that the "additional layer" is bonded to the active face of the moncrystaline silicon substrate layer. Due to a translation error, the bonding was previously recited as "sealed." *See above discussion on Specification amendments.* The Examiner cited Wu's boron/phosphorus doped silicon glass layer as the "sealing" layer. While Wu's layer may present a seal against certain wavelengths of light, it does not provide a bonding between the substrate layer and the additional layer. Wu states that the top cover 18 (which as noted above is not equivalent to Applicant's additional layer) is "deposited" on the glass layer (Wu, Col. 4, Lines 11 – 12). Thus, the glass layer does not perform a bonding function with respect to the top cover 18 and the substrate layer 17. Glass cannot be considered a bonding layer; it merely acts as a substrate for the deposition of the top cover. Furthermore, the interface between the glass layer 51 and silicon substrate layer 17 is not discussed in Wu. Therefore, it cannot be inferred that the glass layer 51 acts as a bonding layer. Accordingly, Wu fails to teach or suggest that the additional layer "is bonded to the active face of the monocrystaline silicon substrate layer by a bonding layer."

For at least these reasons, because Wu fails to teach or suggest at least two elements of Claim 1, Claim 1 is patentable over Wu.

Claim 20

Claim 20 recites similar limitations as Claim 1, and the language of the rejection of Claim 20 is identical to the language of the rejection of Claim 1. Therefore, by virtue of the arguments presented in response to the rejection of Claim 1, Claim 20 is not obvious over Wu.

Claims 5-7, 10, 12-17 and 19

The dependent Claims 5-7 each depend from Claim 1, inherit the limitations thereof, provide further unique and non-obvious combinations, and are patentable over Wu for the reasons given in support of the Claim 1 and by virtue of such further combinations.

Claims 6, 21-23 and 26-28

Claims 6, 21[1] – 23, and 26 - 28 stand rejected under 35 USC 103(a) as being unpatentable over Wu, in view of Kuehnle (US 5,534,056, hereinafter Kuehnle). The Examiner admits that Wu does not teach dopant in the concentration range recited in Claims 6, 22, and 26. The Examiner turns to Kuehnle for the missing teaching and makes the assertion that "it would have been obvious to one of ordinary skill in the art to combine Wu in the range as claimed, because it has been held that where the general conditions of the claims are disclosed in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation." Office Action, Page 4, Line 18 – Page 5, Line 3.

The Examiner's logic is flawed. Wu seeks to shield against UV radiation that may be used to erase EEPROMs. While Wu does state that "the semiconductor material, typically silicon, of substrate 17 blocks ultraviolet light and other radiant energy incident on the bottom of the EPROM device" (Wu, Col. 2, Lines 54 – 57), Wu does not seek to block IR light. The remaining disclosure of Wu does not describe techniques directed to blocking IR light. Therefore, a person of ordinary skill in the art would not look to Wu for how to seek protection against IR radiation. And from that it

[1] Applicants believe the grouping of Claim 21 in this particular rejection is an error. The Examiner is pointing to Kuehnle for recitation of a range of concentration set forth in Claims 66, 22, and 26. Claim 21 does not seem to fit that pattern.

follows that the person of ordinary skill in the art would not be motivated to find teachings on how to modify such a device that is not in any way directed to the hypothetical goal of the person of ordinary skill in the art. Accordingly, a person of ordinary skill in the art would not be motivated to modify Wu with Kuehnle.

The Examiner has made the correct observation that a new use of an old structure is not patentable. However, from that it does not follow that a person of ordinary skill in the art would be motivated to make modifications to that old structure to perfect that new use.

Accordingly, Claims 6, 22, and 26 are patentable over Wu in combination of Kuehnle.

Claims 27 and 28 depend from Claim 26, incorporate all the limitations of Claim 1, and provide further unique and non-obvious combinations, and are patentable over the combination of Wu and Kuehnle for the reasons given in support of Claim 26.

Kuehnle, like Wu, does not teach or suggest the elements of "an additional layer of moncrystaline silicon that is bonded to the active face of the monocrystaline silicon substrate layer by a bonding layer." Therefore, even if the combination of Wu and Kuehnle were considered for the sake of argument, such combination would like the missing elements from Wu. Accordingly, Claim 1 is patentable over the proposed combination of Wu and Kuehnle for this additional reason. Claims 6, 21 and 22 depend from Claim 1, incorporate all the limitations of Claim 1, and provide further unique and non-obvious combinations (e.g., as stated above), and are patentable over the combination of Wu and Kuehnle for this additional reason.

Claims 10, 12, 13, 24, and 29

Claims 10, 12 – 13, 24 and 29 stand rejected 35 USC 103(a) as being unpatentable over Wu, in view of Kobachi, et al., (US 5,811,797, hereinafter Kobachi).

Claims 10, 12, 13 and 24 depend from Claim 1. As argued hereinabove Claim 1 is patentable over Wu because several elements of Claim 1 are missing from the disclosure of Wu. Kobachi also fails to teach or suggest "an additional layer of moncrystaline silicon that is bonded to the active face of the monocrystaline silicon substrate layer by a bonding layer." Therefore, even if Wu and Kobachi were combined, the proposed combination would lack at least these elements from Claim 1. Accordingly, Claim 1 is patentable over the proposed combination of Wu and Kobachi whether the references are taken singly or in combination.

It should further be noted that Wu deals with the protection of a memory cell of a EEPROM device. This is a microscopic structure.

Kobachi deals with a photoreflective detector in which a tilt-angle of an object may be determined. *See e.g.,* Kobachi Figs 1A – Fig 2A and accompanying discussion at Col. 1, Line 17, et seq. Kobachi Figure 1 is reproduced here:

FIG.2A
(PRIOR ART)

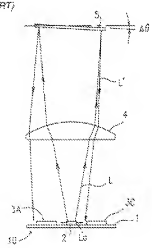
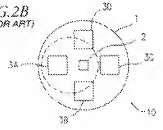


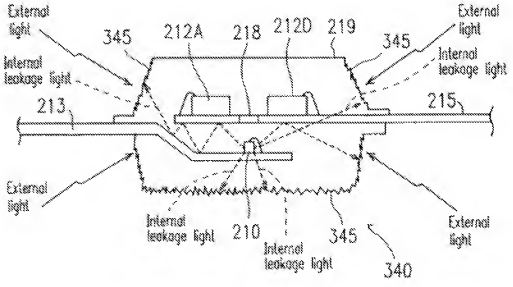
FIG.2B
(PRIOR ART)



It must be appreciated from an examination of Kobachi Figure 1 that this is a very large structure in comparison to the memory cell of Wu. Element 4 is a lens that focus light from a light source 2 and that is reflected back from object 5. The tilt angle of the object may be determined from the image detected by sensors 3. From this it must be quite obvious the Kobachi's device has little in common with the memory cell in a EEPROM.

Kobachi's Figure 22 (cited by the Examiner) shows one embodiment of the photoreflective detector of Kobachi:

FIG. 22



While this detector does have surface irregularities that refract external light, the structure would be applied in a scenario similar to that shown in Figure 1 and is therefore irrelevant to the protection of a microscopic memory cell. A person of ordinary skill in the art of EEPROM memory cells would not look to such gigantic structures to solve problems that are encountered in microscopic devices.

Thus, Wu and Kobachi are from disparate technologies that cannot support a motivation to combine argument.

Kobachi does not teach or suggest a semiconductor package where in "a physical means for providing protection against the action of electromagnetic radiation are formed by surface irregularities" (Claim 10). In fact, Kobachi is not concerned with protection against electromagnetic radiation at all. Kobachi is concerned with the "problem of reduction in S/N

ratio caused by direct light incidence on the light receiving elements…" (Col 3, lines 12-15). While Kobachi does state that "an irregular structure (345) having a plurality of irregularities on the outer surface of the package (219), as the light shielding and absorbing structure, for scattering external light or internal leakage light." (Col 15, lines 4-7), this is no way relates to the Applicant's invention which is aimed at protecting a semiconductor chip from electromagnetic radiation as Kobachi's goal is "a photoreflective detector for improving the S/N ratio as a result of preventing direct light incidence on a light receiving element …" (Col 5, lines 22-24).

Accordingly, a person of ordinary skill would not be motivated to combine Wu and Kobachi. Furthermore, such a combination would lack an element that is applicable to a chip structure. For these reasons, Claims 10, 12 – 13, 24, and 29 are not obvious over the combination of Wu and Kobachi.

Claims 14 – 17, 19, and 30 – 32

Claims 14 – 17, 19 and 30 - 32 stand rejected 35 USC 103(a) as being unpatentable over Wu, in view of Ishikawa (US 5,394,014, hereinafter Ishikawa).

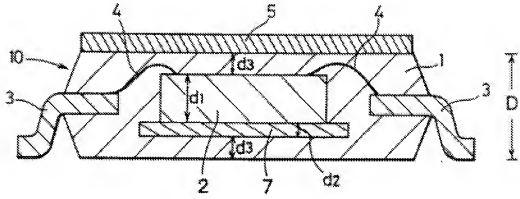
Ishikawa also does not teach or suggest "an additional layer of moncrystaline silicon that is bonded to the active face of the monocrystaline silicon substrate layer by a bonding layer." Therefore the combination of Wu and Ishikawa would lack those elements and Claim 1 would be patentable over the combination.

Claims 14 – 17, and 19 depend from Claim 1 and are patentable over Wu and Ishikawa for at least the reasons given in support of Claim 1.

Ishikawa does not teach or suggest "deposition of metal on the face of the monocrystaline silicon substrate layer that is opposite to the active face." The

Examiner cited Col. 4, Lines 55 – 60. The cited passage describes the construction of the shielding layer 5 of Figure 1 of Ishikawa:

FIG. 1



In Figure 1, "light shielding seal 5 is bonded to the upper surface of the resin package 1." Col. 4, Lines 47 – 48. The element 2 is the semiconductor chip. Col. 4, Lines 42 – 43. Thus, while the light shielding seal 5 may be constructed from metal, it is not deposited on "*the* monocrystaline silicon substrate layer that is opposite to the active face." Claim 30. That would, if at all, be a deposition of a metal layer on a silicon substrate layer deep inside chip 2. Something that is not even hinted at in Ishikawa. Similarly, the additional layer of Claim 14, for example, is bonded to the monocrystaline substrate layer well inside the chip. Thus, Ishikawa's layer 5 cannot be said to be "formed by at least one deposition of metal on the additional layer of moncrystaline silicon."

Accordingly, even if Wu and Ishikawa were combined, the combination would lack at least one element from Claim 30 and 14. Claims 15 -17, and 19 depend from Claim 1 and 14, incorporate the limitations of these claims, provide further unique and non-obvious combinations, and are patentable at least for the reasons given in support of Claims 1 and 14 and by virtue of

such further combinations. Claims 31 and 32 depend from Claim 30, incorporate the limitations of this claim, provide further unique and non-obvious combinations, and are patentable at least for the reasons given in support of Claim 30 and by virtue of such further combinations.

CONCLUSION

It is submitted that all of the claims now in the application are allowable. Applicants respectfully request consideration of the application and claims and its early allowance. If the Examiner believes that the prosecution of the application would be facilitated by a telephonic interview, Applicants invite the Examiner to contact the undersigned at the number given below.

Applicants respectfully request that a timely Notice of Allowance be issued in this application.

Respectfully submitted,

Date: September 28, 2010

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Exhibit A: Polycrystalline Silicon from Wikipedia.org

Polycrystalline silicon

From Wikipedia, the free encyclopedia

Polycrystalline silicon, also called polysilicon, is a material consisting of small silicon crystals. It differs from single-crystal silicon, used for electronics and solar cells, and from amorphous silicon, used for thin film devices and solar cells.

Contents

- 1 Single crystalline vs polycrystalline silicon
- 2 Polycrystalline silicon components
  - 2.1 Solar panel and applications
- 3 Deposition methods
- 4 Upgraded metallurgical-grade silicon
- 5 Manufacturers
  - 5.1 Polysilicon
- 6 Printed electronics
- 7 See also
- 8 References
- 9 External links

Single crystalline vs polycrystalline silicon

In single crystal silicon, the crystalline framework is homogenous, which can be recognized by an even external coloring.[1] In single crystal silicon, also called monocrystal, the crystal lattice of the entire sample is continuous and unbroken with no grain boundaries. Large single crystals are exceedingly rare in nature and can also be difficult to produce in the laboratory (see also recrystallisation). In contrast an amorphous structure where the atomic position is limited to short range order.

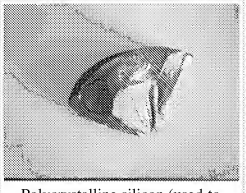
Polycrystalline and *paracrystalline* phases (see Polycrystal) are composed of a number of smaller crystals or *crystallites*. Polycrystalline silicon (or semicrystalline silicon, polysilicon, poly-Si, or simply "poly") is a material consisting of multiple small silicon crystals. Polycrystalline cells can be recognized by a visible grain, a "metal flake effect". Semiconductor grade (also solar grade) polycrystalline silicon is

converted to "single crystal" silicon – meaning that the randomly associated crystallites of silicon in "polycrystalline silicon" are converted to a large "single" crystal. Single crystal silicon is used to manufacture most Si-based microelectronic devices. Polycrystalline silicon can be as much as 99.9999% pure.[2] Ultra-pure poly is used in the semiconductor industry, starting from poly rods that are five to eight feet in length. In microelectronic industry (semiconductor industry), poly is used both at the macro-scale and micro-scale (component) level. Single crystals are grown using the Czochralski process, float-zone and Bridgman techniques.

A rod of semiconductor-grade polysilicon (held by Leo Rogers of Polycrystalline Silicon Technology Corporation (P.S.T.).

Polycrystalline silicon components

Polysilicon is a key component for integrated circuit and central processing unit manufacturers such as AMD and Intel. At the component level, polysilicon has long been used as the conducting gate material in MOSFET and CMOS processing technologies. For these technologies it is deposited using low-pressure chemical-vapour deposition (LPCVD) reactors at high temperatures and is usually heavily doped n-type or p-type.

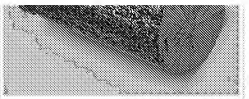


Polycrystalline silicon (used to produce silicon monocrystals by Czochralski process)

More recently, intrinsic and doped polysilicon is being used in large-area electronics as the active and/or doped layers in thin-film transistors. Although it can be deposited by LPCVD, plasma-enhanced chemical vapour deposition (PECVD), or solid-phase crystallization (SPC) of amorphous silicon in certain processing regimes, these processes still require relatively high temperatures of at least 300 °C. These temperatures make deposition of polysilicon possible for glass substrates but not for plastic substrates. The deposition of polycrystalline silicon on plastic substrates is motivated by the desire to be able to manufacture digital displays on flexible screens. Therefore, a relatively new technique called laser crystallization has been devised to crystallize a precursor amorphous silicon (a-Si) material on a plastic substrate without melting or damaging the plastic. Short, high-intensity ultraviolet laser pulses are used to heat the deposited a-Si material to above the melting point of silicon, without melting the entire substrate. The molten silicon will then crystallize as it cools. By precisely controlling the temperature gradients, researchers have been able to grow very large grains, of up to hundreds of micrometers in size in the extreme case, although grain sizes of 10 nanometers to 1 micrometer are also common. In order to create devices on polysilicon over large-areas however, a crystal grain size smaller than the device feature size is needed for homogeneity of the devices. Another method to produce poly-Si at low temperatures is metal-induced crystallization where an amorphous-Si thin film can be crystallized at temperatures as low as 150C if annealed while in contact of another metal film such as aluminium, gold, or silver.

Polysilicon has many applications in VLSI manufacturing. One of its primary uses is as gate electrode material for MOS devices. A polysilicon gate's electrical conductivity may be increased by depositing a metal (such as tungsten) or a metal silicide (such as tungsten silicide) over the gate. Polysilicon may also be employed as a resistor, a

conductor, or as an ohmic contact for shallow junctions, with the desired electrical conductivity attained by doping the polysilicon material.


A polycrystalline silicon rod made by the Siemens process

One major difference between polysilicon and a-Si is that the mobility of the charge carriers of the polysilicon can be orders of magnitude larger and the material also shows greater stability under electric field and light-induced stress. This allows more complex, high-speed circuity to be created on the glass substrate along with the a-Si devices, which are still needed for their low-leakage characteristics. When polysilicon and a-Si devices are used in the same process this is called hybrid processing. A complete polysilicon active layer process is also used in some cases where a small pixel size is required, such as in projection displays.

Solar panel and applications

Main article: Solar panel

Polycrystalline silicon is also a key component of solar panel construction. Growth of the photovoltaic solar industry is limited by the supply of the polysilicon material.[3] For the first time, in 2006, over half of the world's supply of polysilicon is being used for production of renewable electricity solar power panels.[4] Only twelve factories are known to produce solar-grade polysilicon in 2008. Monocrystalline silicon is higher priced and more efficient than multicrystalline.

Deposition methods

Polysilicon deposition, or the process of depositing a layer of polycrystalline silicon on a semiconductor wafer, is achieved by pyrolyzing silane (SiH_4) at 580 to 650 °C. This pyrolysis process releases hydrogen.

Polysilicon layers can be deposited using 100% silane at a pressure of 25–130 Pa (0.2 to 1.0 Torr) or with 20–30% silane (diluted in nitrogen) at the same total pressure. Both of these processes can deposit polysilicon on 10–200 wafers per run, at a rate of 10–20 nm/min and with thickness uniformities of ±5%. Critical process variables for polysilicon deposition include temperature, pressure, silane concentration, and dopant concentration. Wafer spacing and load size have been shown to have only minor effects on the deposition process. The rate of polysilicon deposition increases rapidly with temperature, since it follows Arrhenius behavior, that is deposition rate = $A \cdot \exp(-qE_a/kT)$ where q is electron charge and k is the Boltzmann constant. The activation energy (E_a) for polysilicon deposition is about 1.7 eV. Based on this equation, the rate of polysilicon deposition increases as the deposition temperature increases. There will be a minimum temperature, however, wherein the rate of deposition becomes faster than the rate at which unreacted silane arrives at the surface. Beyond this temperature, the deposition rate can no longer increase with temperature, since it is now being hampered by lack of silane from which the polysilicon will be generated. Such a reaction is then said to be 'mass-transport-limited.' When a polysilicon deposition process becomes mass-transport-limited, the reaction rate becomes dependent primarily on reactant concentration, reactor geometry, and gas flow.

When the rate at which polysilicon deposition occurs is slower than the rate at which unreacted silane arrives, then it is said to be surface-reaction-limited. A deposition process that is surface-reaction-limited is primarily dependent on reactant concentration and reaction temperature. Deposition processes must be surface-reaction-limited because they result in excellent thickness uniformity and step coverage. A plot of the logarithm of the deposition rate against the reciprocal of the absolute temperature in the surface-reaction-limited region results in a straight line whose slope is equal to $-qE_a/k$.

At reduced pressure levels for VLSI manufacturing, polysilicon deposition rate below 575 °C is too slow to be practical. Above 650 °C, poor deposition uniformity and excessive roughness will be encountered due to unwanted gas-phase reactions and silane depletion. Pressure can be varied inside a low-pressure reactor either by changing the pumping speed or changing the inlet gas flow into the reactor. If the inlet gas is composed of both silane and nitrogen, the inlet gas flow, and hence the reactor pressure, may be varied either by changing the nitrogen flow at constant silane flow, or changing both the nitrogen and silane flow to change the total gas flow while keeping the gas ratio constant.

Polysilicon doping, if needed, is also done during the deposition process, usually by adding phosphine, arsine, or diborane. Adding phosphine or arsine results in slower deposition, while adding diborane increases the deposition rate. The deposition thickness uniformity usually degrades when dopants are added during deposition.

Upgraded metallurgical-grade silicon

Upgraded metallurgical-grade (UMG) silicon (also known as UMG Si) solar cell was created to close the efficiency gap between industrial multicrystalline and high-efficiency monocrystalline silicon cell. UMG silicon, which is three orders of magnitude less pure than polysilicon, is being researched and considered as a cost-effective alternative to polysilicon.[5]

A project is targeting 18–22% efficient cells (upgraded metallurgical silicon could potentially reach efficiencies of only 0.5% less than polysilicon), at manufacturing costs of less than $1 per peak watt.

A project is also attempting to build 1,000 tons of UMG silicon capacity for $15 million in six months.[6]

SolarWorld has established a joint venture with Scheuten Solarholding to turn dirty metallurgical-grade silicon into high-purity solar-grade silicon.[7]

Manufacturers

Polysilicon

Polysilicon manufacturing market is in a very fast change now (2010). With high spot-prices in 2008/2009 and lack of available material, many companies announced additional capacities for the coming years. Established producers (mentioned below) expand their capacities, additionally newcomers – especially from Asia – are moving into this

market. Even long-time players in the field had difficulties recently to ramp-up new plants. It is yet unclear which companies will be able to produce at costs low enough to be profitable after the steep drop in spot-prices of the last months.[8][9]


Chemical processing equipment at a P.S.T. poly-silicon plant

Leading producers as of 2010 are:

- *Hemlock Semiconductor* (capacity 2010: 36 kt) [10] from USA
- *Wacker Chemie* (capacity 2010: 25 kt)[11] from Germany,
- *GCL-Poly* (capacity 2010: 18kt)[12] from Hongkong,
- *OCI* (capacity 2010: 17 kt)[13] from South Korea,
- *MEMC Electronic Materials* (capacity 2010: 8)[14] from USA,
- *Renewable Energy Corporation ASA (REC)* (capacity 2010: 17kt)[15] from Norway and
- *Tokuyama* (capacity 2010: 8,2 kt)[16] from Japan.

Printed electronics

Main article: Printed electronics

Micro-tec has introduced an automated multi-layer print system for crystalline solar cells.[17]

See also

- Bulk
- Cadmium telluride
- Low-cost solar cell
- Metallurgical grade silicon
- Nanocrystalline silicon
- Polycrystal
- Photovoltaic cells
- Photovoltaic module
- Wafer (electronics)

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